

**WHAT IS CLAIMED IS:**

1. A method of depositing a coating, comprising:  
providing a substrate; and  
thermally spraying a ceramic powder comprising a garnet crystal structure, to  
form a coating on the substrate, the coating comprising a garnet crystal  
structure phase.
2. The method of claim 1, wherein the powder comprises  $M_3Al_5O_{12}$  having  
the garnet crystal structure, wherein M consists of at least one element from the group  
consisting of yttrium, scandium, lanthanide series elements, and combinations thereof.
3. The method of claim 2, wherein M includes at least yttrium.
4. The method of claim 3, wherein M includes yttrium and not greater than 20  
mol% of scandium, a lanthanide series element, and combinations thereof, of the total  
amount of M.
5. The method of claim 4, wherein M includes yttrium and neodymium.
6. The method of claim 3, wherein the powder consists essentially of yttrium  
aluminum garnet (YAG).
7. The method of claim 6, wherein the powder is stoichiometric yttrium  
aluminum garnet.
8. The method of claim 6, wherein the powder is rich in yttrium content  
relative to stoichiometric YAG.
9. The method of claim 1, wherein the powder consists essentially of  
 $M_3Al_5O_{12}$  having the garnet crystal structure, wherein M consists of at least one  
element from the group consisting of yttrium, scandium, lanthanide series elements,  
and combinations thereof.

10. The method of claim 1, wherein the substrate is metal.
11. The method of claim 10, wherein the substrate contains at least one element from the group consisting of molybdenum, tungsten, iron, nickel, aluminum, and titanium.
12. The method of claim 11, wherein the substrate comprises an aluminum alloy.
13. The method of claim 11, wherein the substrate comprises a stainless steel alloy.
14. The method of claim 1, wherein the substrate is a semiconductor processing component.
15. The method of claim 1, wherein the substrate comprises a non-metal.
16. The method of claim 15, wherein the substrate comprises silicon.
17. The method of claim 15, wherein the substrate comprises a ceramic.
18. The method of claim 15, wherein the substrate comprises a material selected from the group consisting of alumina and silica
19. The method of claim 1, wherein the predominant phase of the coating is said garnet crystal structure.
20. The method of claim 19, wherein the coating comprises  $M_3Al_5O_{12}$  having the garnet crystal structure, wherein M consists of at least one element from the group consisting of yttrium, scandium, lanthanide series elements, and combinations thereof.
21. The method of claim 20, wherein M includes at least yttrium.

22. The method of claim 21, wherein M includes yttrium and not greater than 20 mol% of scandium, a lanthanide series element, and combinations thereof, of the total amount of M.

23. The method of claim 22, wherein M includes yttrium and neodymium.

24. The method of claim 21, wherein M includes yttrium and not greater than 20 mol% of scandium, a lanthanide series element, and combinations thereof, of the total amount of M.

25. The method of claim 21, wherein the coating consists essentially of yttrium aluminum garnet (YAG).

26. The method of claim 25, wherein the coating is stoichiometric yttrium aluminum garnet.

27. The method of claim 25, wherein the coating is rich in yttrium content relative to stoichiometric YAG.

28. The method of claim 19, wherein the coating consists essentially of  $M_3Al_5O_{12}$  having the garnet crystal structure, wherein M consists of at least one element from the group consisting of yttrium, scandium, lanthanide series elements, and combinations thereof.

29. The method of claim 19, wherein the coating has a maximum peak height of crystalline phases other than said garnet crystal structure phase that is less than 10% of the maximum peak height of the garnet crystal structure phase.

30. The method of claim 1, wherein the coating comprises said garnet crystal structure as deposited by thermal spraying, without any post-deposition heat treatment steps.

31. The method of claim 1, wherein the substrate is preheated prior to thermal spraying.

32. The method of claim 31, wherein the substrate is preheated to a temperature of at least about 150°C.

33. The method of claim 1, wherein thermal spraying is carried out by supplying the ceramic powder to a plasma torch.

34. A coated article, comprising:

a substrate; and

a coating overlying the substrate, the coating having a thickness greater than about 10 microns and comprising a garnet crystal structure, wherein the substrate has a coefficient of thermal expansion at least about 30% greater than or less than a thermal expansion coefficient of the coating.

35. The article of claim 34, wherein the substrate is metal, and comprises at least one element from the group consisting of molybdenum, tungsten, iron, nickel, aluminum, and titanium.

36. The article of claim 35, wherein the substrate comprises an iron-based or nickel-based superalloy.

37. The article of claim 35, wherein the substrate comprises a stainless steel alloy.

38. The article of claim 35, wherein the substrate comprises an aluminum alloy.

39. The article of claim 34, wherein the substrate comprises a non-metal.

40. The article of claim 39, wherein the substrate comprises silicon.

41. The article of claim 39, wherein the substrate comprises a ceramic.

42. The article of claim 39 wherein the substrate is selected from a group consisting of silica and alumina.

43. The article of claim 34, wherein the coating has a thickness of at least about 50 microns.

44. The article of claim 34, wherein the coating has a thickness at least about 100 microns.

45. The article of claim 34, wherein the predominant phase of the coating is said garnet crystal structure.

46. A semiconductor processing tool, comprising:  
a substrate; and  
a coating overlying the substrate, the coating being formed by thermal spraying a ceramic powder comprising a garnet crystal structure, whereby the coating comprises a garnet crystal structure phase.

47. The tool of claim 46, wherein the processing tool is selected from the group consisting of a deposition apparatus, a diffusion apparatus, an etch apparatus, a chemical mechanical polishing apparatus, and annealing apparatus.

48. The tool of claim 47, wherein the processing tool is an etch apparatus.

49. The tool of claim 48, wherein the etch apparatus includes an etching chamber defined by a base upon which is disposed a lid, the etch apparatus including an electrostatic chuck disposed in the chamber for holding a semiconductor wafer.

50. The tool of claim 49, wherein the substrate includes at least one of the base, the lid, and the electrostatic chuck.

51. The tool of claim 49, wherein the etch apparatus further includes focus ring disposed in the chamber, positioned to surround a semiconductor wafer, and a liner, wherein the electrostatic chuck is disposed radially within the liner.

52. The tool of claim 51, wherein the substrate includes at least one of the ring and the liner.

53. The tool of claim 49, wherein the lid is in the form of a dome.

54. A semiconductor processing tool, comprising:

a substrate; and

a coating overlying the substrate, the coating having a thickness greater than about 10 microns and comprising a garnet crystal structure, wherein the substrate has a coefficient of thermal expansion at least about 30% greater than or less than a thermal expansion coefficient of the coating.

55. A method for forming semiconductor devices, comprising:

providing a silicon wafer;

exposing the silicon wafer to a series of processing steps to form plurality of semiconductor die areas, the processing steps including a step of placing the wafer in a processing chamber of a processing tool, a component of which has a ceramic coating thereon comprising a garnet crystal phase; and

dicing the wafer into a plurality of semiconductor die.

56. The method of claim 55, wherein the processing tool is selected from the group consisting of a deposition apparatus, a diffusion apparatus, an etch apparatus, a chemical mechanical polishing apparatus, and annealing apparatus.

57. The method of claim 56, wherein the processing tool is an etch apparatus.

58. The method of claim 57, wherein the etch apparatus includes an etching chamber defined by a base upon which is disposed a lid, the etch apparatus including an electrostatic chuck disposed in the chamber for holding a semiconductor wafer.

59. The method of claim 58, wherein the component on which the coating is disposed includes at least one of the base, the lid, and the electrostatic chuck.

60. The method of claim 58, wherein the etch apparatus further includes a focus ring disposed in the chamber, positioned to surround a semiconductor wafer, and a liner, wherein the electrostatic chuck is disposed radially within the liner.

61. The method of claim 60, wherein the component on which the coating is disposed includes at least one of the focus ring and the liner.

62. The method of claim 55, further comprising a step of packaging the semiconductor die to form a packaged semiconductor device.

63. The method of claim 55, wherein the ceramic coating is provided on a surface of the component, the surface being formed of a material having a coefficient of thermal expansion at least about 30% greater than or less than a thermal expansion coefficient of the coating.

64. The method of claim 55, wherein the coating is formed by thermal spraying a ceramic powder comprising a garnet crystal structure, whereby the coating comprises a garnet crystal structure phase.